

20A, 600V N-CHANNEL MOSFET

GENERAL DESCRIPTION

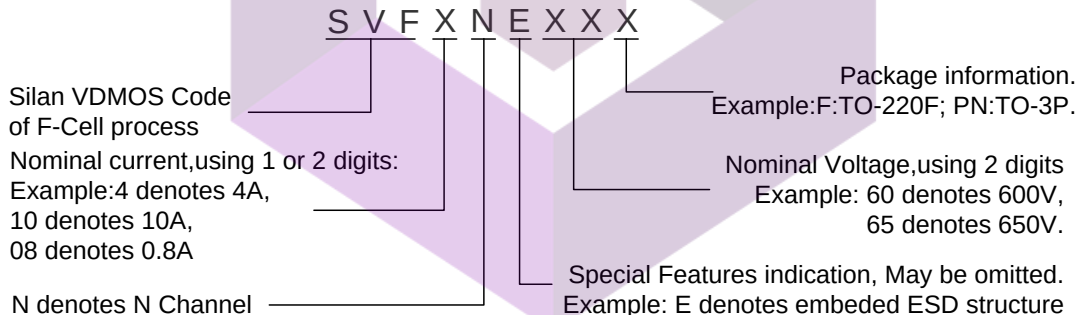
SVF20N60F/PN is an N-channel enhancement mode power MOS field effect transistor which is produced using Silan proprietary F-Cell™ structure VDMOS technology. The improved planar stripe cell and the improved guard ring terminal have been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are widely used in AC-DC power suppliers, DC-DC converters and H-bridge PWM motor drivers.

FEATURES

- 20A, 600V, $R_{DS(on)(typ.)} = 0.28\Omega @ V_{GS} = 10V$
- Low gate charge
- Low C_{rss}
- Fast switching
- Improved dv/dt capability

NOMENCLATURE



ORDERING INFORMATION

Part No.	Package	Marking	Hazardous Substance Control	Packing
SVF20N60F	TO-220F-3L	SVF20N60F	Pb free	Tube
SVF20N60PN	TO-3P	20N60	Pb free	Tube

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ABSOLUTE MAXIMUM RATINGS (T_c=25°C unless otherwise noted)

Characteristics		Symbol	Ratings		Unit
			SVF20N60F	SVF20N60PN	
Drain-Source Voltage		V _{DS}	600		V
Gate-Source Voltage		V _{GS}	±30		V
Drain Current	T _C =25°C	I _D	20.0		A
	T _C =100°C		12.6		
Drain Current Pulsed		I _{DM}	80.0		A
Power Dissipation(T _C =25°C)		P _D	74	258	W
-Derate above 25°C			0.59	2.06	W/°C
Single Pulsed Avalanche Energy(Note 1)		E _{AS}	1433		mJ
Operation Junction Temperature Range		T _J	-55~+150		°C
Storage Temperature Range		T _{stg}	-55~+150		°C

THERMAL CHARACTERISTICS

Characteristics	Symbol	Ratings		Unit
		SVF20N60F	SVF20N60PN	
Thermal Resistance, Junction-to-Case	R _{θJC}	1.69	0.48	°C/W
Thermal Resistance, Junction-to-Ambient	R _{θJA}	62.5	50	°C/W

ELECTRICAL CHARACTERISTICS (T_c=25°C unless otherwise noted)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Drain -Source Breakdown Voltage	B _{VDS}	V _{GS} =0V, I _D =250μA	600	--	--	V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V	--	--	1.0	μA
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±30V, V _{DS} =0V	--	--	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{GS} = V _{DS} , I _D =250μA	2.0	--	4.0	V
Static Drain- Source On State Resistance	R _{DS(on)}	V _{GS} =10V, I _D =10.0A	--	0.28	0.35	Ω
Input Capacitance	C _{iss}	V _{DS} =25V, V _{GS} =0V, f=1.0MHz	--	2708	--	pF
Output Capacitance	C _{oss}		--	293	--	
Reverse Transfer Capacitance	C _{rss}		--	6.6	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} =300V, I _D =20.0A, R _G =25Ω, (Note2,3)	--	27.0	--	ns
Turn-on Rise Time	t _r		--	44.0	--	
Turn-off Delay Time	t _{d(off)}		--	82.0	--	
Turn-off Fall Time	t _f		--	44.4	--	
Total Gate Charge	Q _g	V _{DS} =480V, I _D =20.0A, V _{GS} =10V, (Note 2,3)	--	47.45	--	nC
Gate-Source Charge	Q _{gs}		--	14.13	--	
Gate-Drain Charge	Q _{gd}		--	14.51	--	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Continuous Source Current	I_S	Integral Reverse P-N Junction	--	--	20.0	A
Pulsed Source Current	I_{SM}	Diode in the MOSFET	--	--	80.0	
Diode Forward Voltage	V_{SD}	$I_S=20.0A, V_{GS}=0V$	--	--	1.4	V
Reverse Recovery Time	T_{rr}	$I_S=20.0A, V_{GS}=0V,$	--	630.1	--	ns
Reverse Recovery Charge	Q_{rr}	$di_F/dt=100A/\mu s$ (Note 2)	--	8.19	--	μC

Notes:

1. $L=30mH, I_{AS}=9.45A, V_{DD}=100V, R_G=25\Omega$, starting $T_J=25^\circ C$;
2. Pulse Test: Pulse width $\leq 300\mu s$, Duty cycle $\leq 2\%$;
3. Essentially independent of operating temperature.

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TYPICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

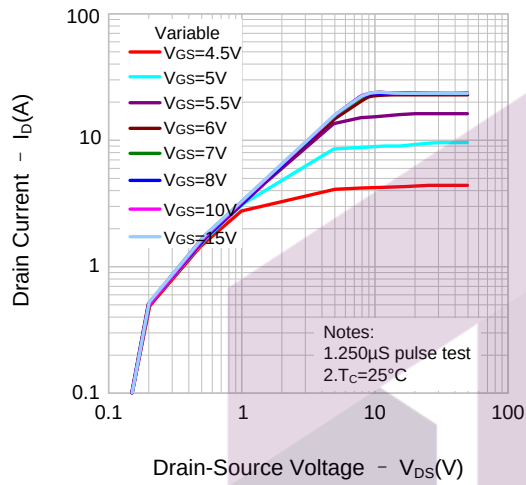


Figure 2. Transfer Characteristics

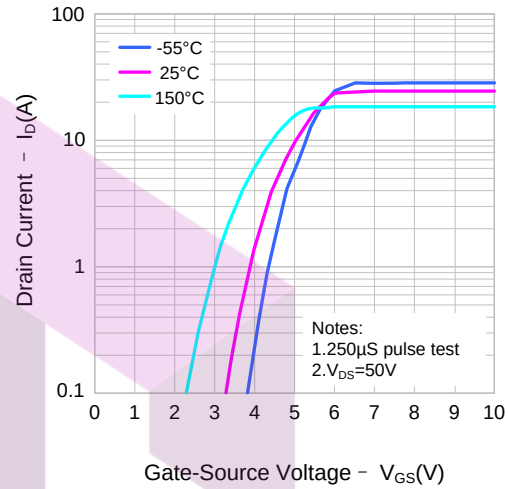


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

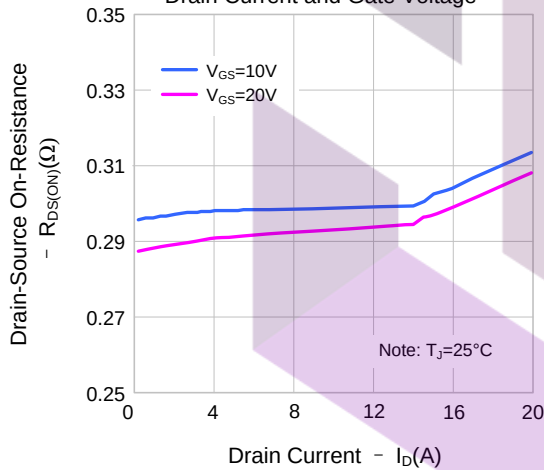


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

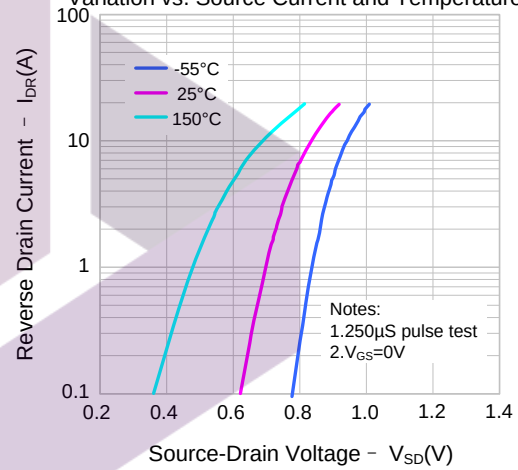


Figure 5. Capacitance Characteristics

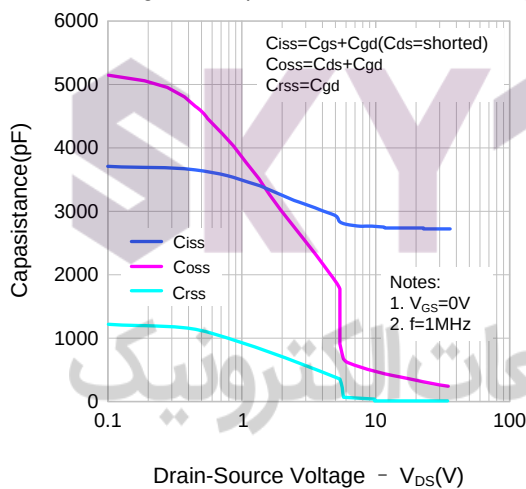
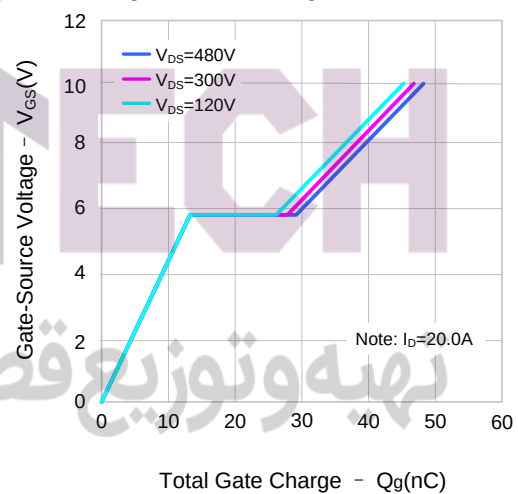


Figure 6. Gate Charge Characteristics



TYPICAL CHARACTERISTICS(continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

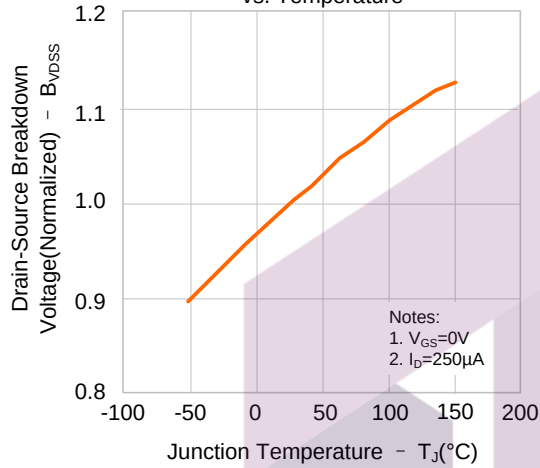


Figure 8. On-resistance Variation vs. Temperature

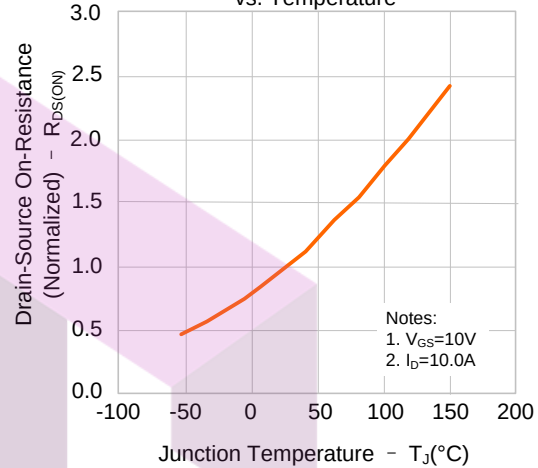


Figure 9-1. Max. Safe Operating Area(SVF20N60F)

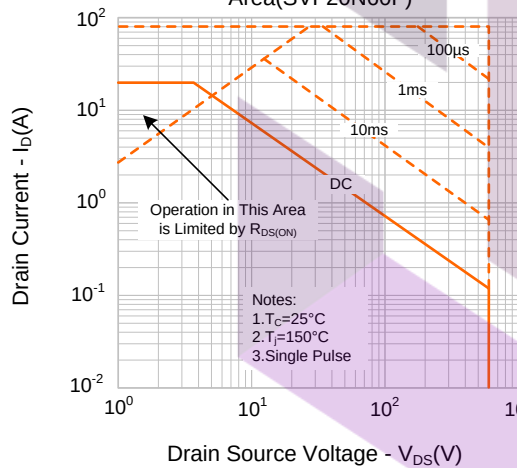


Figure 9-2. Max. Safe Operating Area(SVF20N60PN)

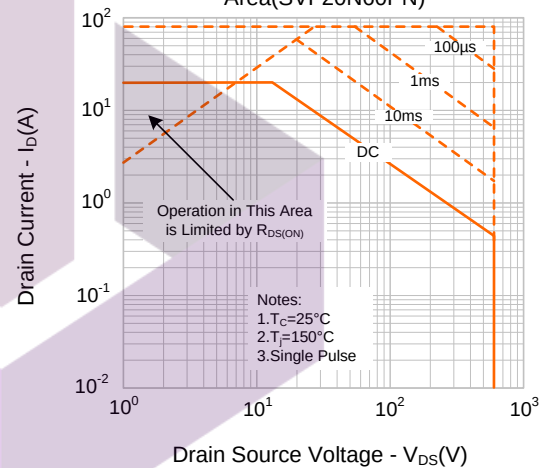
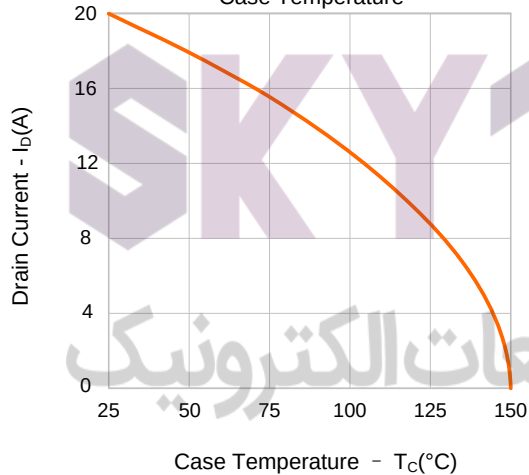
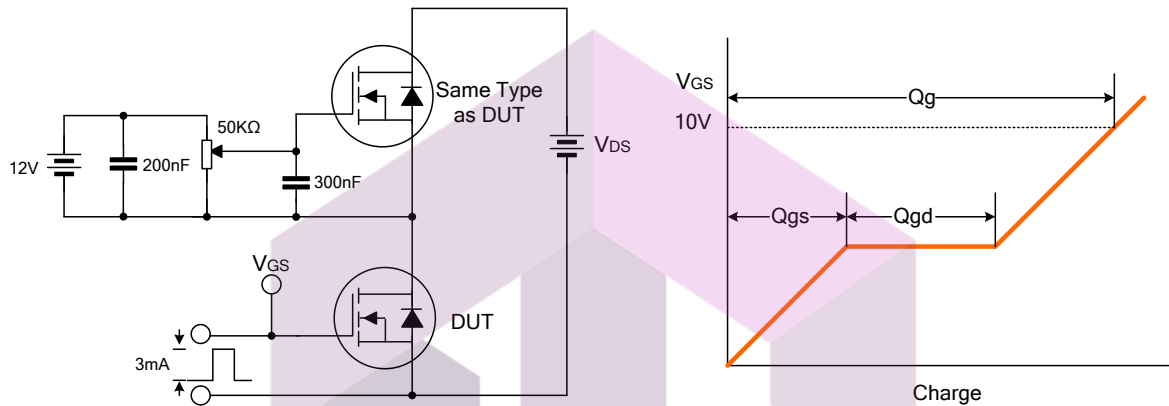


Figure 10. Maximum Drain Current vs. Case Temperature

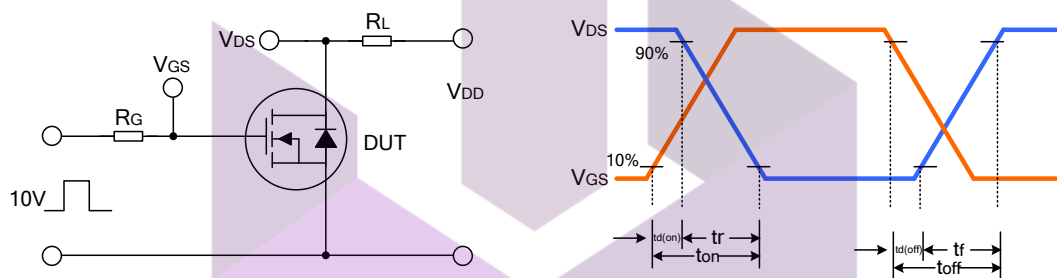


TYPICAL TEST CIRCUIT

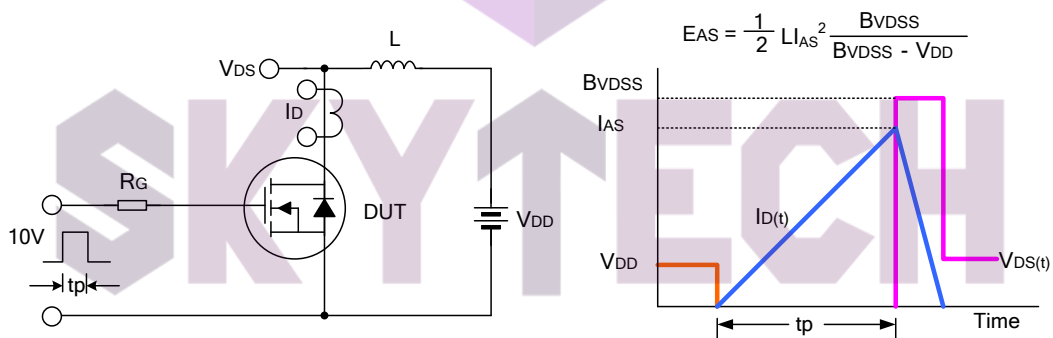
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform

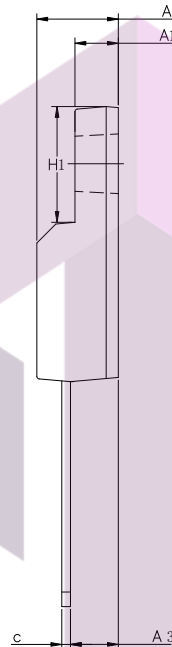
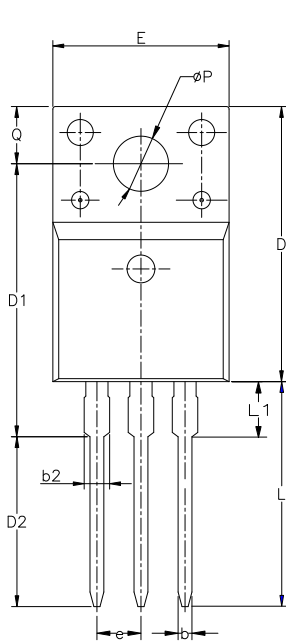


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PACKAGE OUTLINE

TO-220F-3L

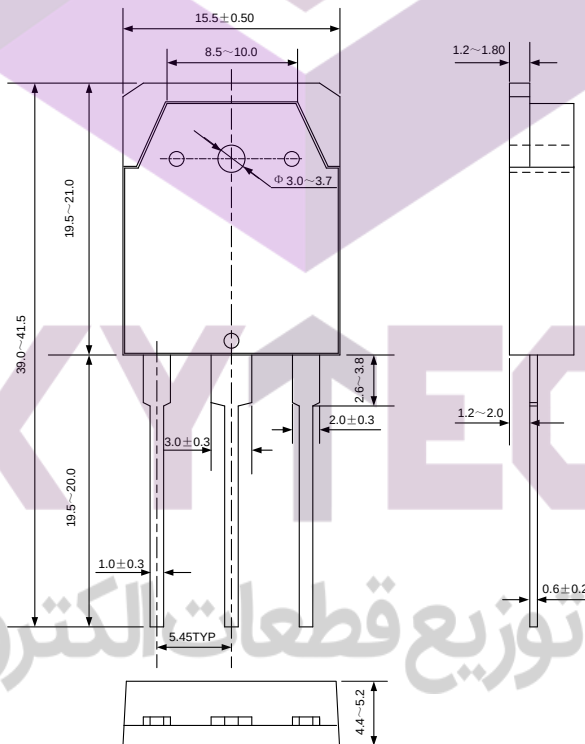
UNIT: mm



SYMBOL	MIN	NOM	MAX
A	4.42	4.70	5.02
A1	2.30	2.54	2.80
A3	2.50	2.76	3.10
b	0.70	0.80	0.90
b2	—	—	1.47
c	0.35	0.50	0.65
D	15.25	15.87	16.25
D1	15.30	15.75	16.30
D2	9.30	9.80	10.30
E	9.73	10.16	10.36
e	2.54BCS		
H1	6.40	6.68	7.00
L	12.48	12.98	13.48
L1	/	/	3.50
ØP	3.00	3.18	3.40
Q	3.05	3.30	3.55

TO-3P

UNIT: mm



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Part No.:	SVF20N60F/PN	Document Type:	Datasheet
Copyright:	HANGZHOU SILAN MICROELECTRONICS CO.,LTD	Website:	http://www.silan.com.cn
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Revision History:	1. Modify the EAS test condition.		
Rev.:	1.5	Author:	Yin Zi
Revision History:	1. Modify the package information of TO-220F-3L		
Rev.:	1.4	Author:	Yin Zi
Revision History:	1. Modify the thermal characteristics		
Rev.:	1.3	Author:	Zhang Kefeng
Revision History:	1. Modify the ordering information		
Rev.:	1.2	Author:	Zhang Kefeng
Revision History:	1. Change the schematic diagram of MOS		
Rev.:	1.1	Author:	Zhang Kefeng
Revision History:	1. Add the package of TO-3PN		
Rev.:	1.0	Author:	Zhang Kefeng
Revision History:	1. Initial release		

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